CLAIMS

The following listing of claims replaces all prior versions:

1. (currently amended) A bit error detection circuit comprising:

a predictor circuit that uses a plurality of bits of a bit sequence to predict a next bit in the sequence;

a comparator circuit that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit; and

a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit~~, regardless of the statistical distribution of erroneous bits in the bit sequence~~; and

a trigger circuit that, in response to an error in the actual next bit indicating presence of an erroneous bit in the predictor circuit, disables the correction circuit until the predictor circuit no longer contains erroneous bits.

2. (original) A bit error detection circuit as in claim 1 wherein the correction circuit comprises a circuit element that replaces the actual next bit with the corrected actual next bit in the plurality of bits.

3. (original) A bit error detection circuit as in claim 1 wherein the bit sequence comprises a pseudo-random bit sequence and the predictor circuit predicts the next bit by comparing two of the bits of the sequence.

4. (canceled)

5. (currently amended) A bit error detection circuit as in ~~claim 4~~ claim 1 wherein the trigger circuit determines that the predictor circuit no longer contains erroneous bits by determining ~~activates the correction circuit~~ when no erroneous bits have been observed during a predefined interval.

6. (original) A bit error detection circuit as in claim 5 wherein the predefined interval is

defined in terms of a quantity of bits.

7. (original) A bit error detection circuit as in claim 5 wherein the predefined interval is defined in terms of an interval of time.

8. (currently amended) A bit error detection circuit comprising:

a shift register that receives N bits of a pseudo-random bit sequence (PRBS);

a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted (N+1)-th bit;

a second logic element that receives the signal indicative of the predicted (N+1)-th bit and a signal indicative of an actual (N+1)-th bit and provides an output signal indicative of any error in the actual (N+1)-th bit; and

a third logic element that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register; and

a trigger circuit that, in response to an error in the actual (N+1)-th bit indicating presence of an erroneous bit in the shift register, disables the third logic element from correcting the actual (N+1)-th bit until the shift register no longer contains erroneous bits.

9. (original) A bit error detection circuit as in claim 8 wherein the third logic element receives the actual (N+1)-th bit from one of the shift register stages, corrects said bit according to the output signal, and inserts said bit as corrected into another one of the shift register stages in place of the actual (N+1)-th bit.

10. (canceled)

11. (currently amended) A bit error detection circuit as in ~~claim 10~~ claim 8 wherein the trigger circuit comprises a logic circuit that receives the output signal and provides an enabling signal if no error is indicated while a predefined number of bits propagates through the shift register.

12. (currently amended) A bit error detection circuit as in ~~claim 10~~ claim 8 wherein the

trigger circuit comprises a timer that provides an enabling signal if no error is indicated during a predefined time interval.

13. (canceled)

14. (currently amended) A method of detecting errors in a bit sequence comprising:

predicting a next bit of a bit sequence according to a plurality of previous bits of the sequence;

comparing the predicted bit with an actual next bit; and

if the comparison indicates a difference between the predicted and actual next bits, providing an error signal and correcting the actual next bit~~, regardless of the statistical distribution of erroneous bits in the bit sequence~~; and

in response to the error signal, disabling correcting the actual next bit until no additional error signal has been provided during a predefined interval.

15. (original) A method as in claim 14 wherein correcting the actual next bit comprises replacing the actual next bit with the corrected actual next bit in the bit sequence.

16. (original) A method as in claim 14 wherein the bit sequence comprises a pseudo-random bit sequence.

17. (canceled)

18. (canceled)

19. (currently amended) A method as in ~~claim 18 and further comprising~~ claim 14 wherein disabling correcting the actual next bit comprises measuring a period of time to determine when the predefined interval has elapsed.

20. (currently amended) A method as in ~~claim 18 and further comprising~~ claim 14 wherein disabling correcting the actual next bit comprises counting a predefined number of bits as

they propagate through a circuit element to determine when the predefined interval has elapsed.

21. (currently amended) A bit error detector comprising:

an actual next bit input that receives a plurality of bits of a bit sequence;

a predictor coupled to the input and having a predicted next bit output;

a comparator coupled to the predicted next bit output and to the actual next bit input, the comparator having an error signal output; and

a corrector coupled to the error signal output and having a corrected actual next bit output

~~a means for detecting errors in the bit sequence, regardless of the statistical distribution of erroneous bits in the bit sequence~~; and

means for disabling the corrector, in response to an error signal indicating presence of an erroneous bit in the predictor, from correcting the actual next bit until the predictor no longer contains erroneous bits.

22. (previously presented) A bit error detector as in claim 21 wherein:

the predictor comprises a predictor circuit for receiving the plurality of bits, for determining a predicted next bit from at least some of the plurality of bits, and for providing the predicted next bit at the predicted next bit output;

the comparator comprises a comparator circuit for receiving the predicted next bit and the actual next bit, for comparing the predicted next bit and the actual next bit, and for providing an error signal at the error signal output when a difference is detected between the predicted next bit and the actual next bit; and

the corrector comprises a correction circuit for receiving the error signal, producing a corrected actual next bit, and providing a corrected actual next bit, and providing the corrected actual next bit at the corrected actual next output.

23. (currently amended) A high-speed communication system, comprising:

a pseudo-random bit sequence generator for creating a pseudo-random bit sequence;

a transmitter in signal communication with the pseudo-random bit sequence generator,

wherein an input to the transmitter is an output of the pseudo-random sequence generator;

a communication channel in signal communication with the transmitter, the transmitter for transmitting the pseudo-random bit sequence over the communication channel; and

a pseudo-random bit sequence error detector, in signal communication with the communications channel, for detecting and correcting any error in an actual next bit of the pseudo-random bit sequence, wherein the pseudo-random bit sequence error detector comprises:

a predictor circuit that uses a plurality of bits of the pseudo-random bit sequence to provide a predicted next bit of the pseudo-random bit sequence;

a comparator circuit that compares the actual next bit in the pseudo-random bit sequence with the predicted next bit to determine whether there is an error in the actual next bit; and

a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit~~, regardless of the statistical distribution of erroneous bits in the bit sequence~~; and

a trigger circuit that, in response to an error in the actual next bit indicating presence of an erroneous bit in the predictor circuit, disables the correction circuit until the predictor circuit no longer contains erroneous bits.